

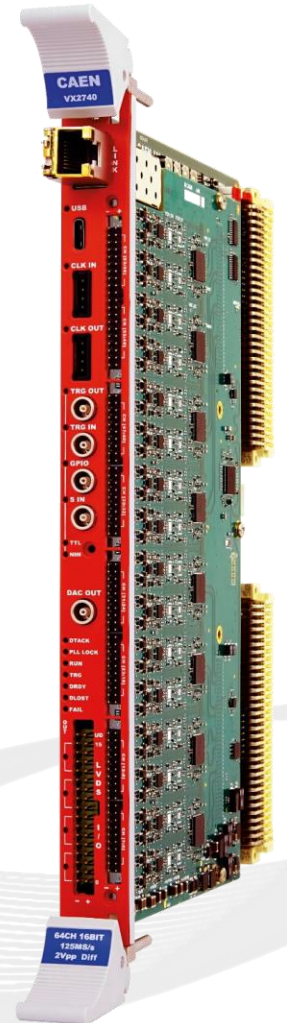


Second School on Waveform Digitizer

Alberto Potenza
Bruno Angelucci
Matteo Bianchini

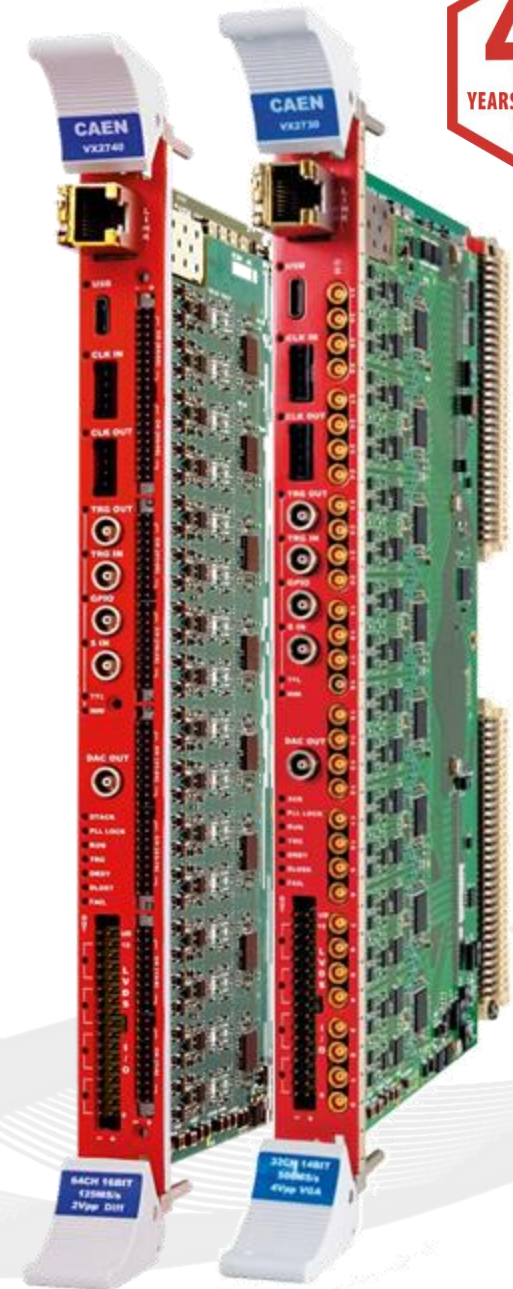
Overview

- What's New
- Firmware Description
- Hands-On
- Questions



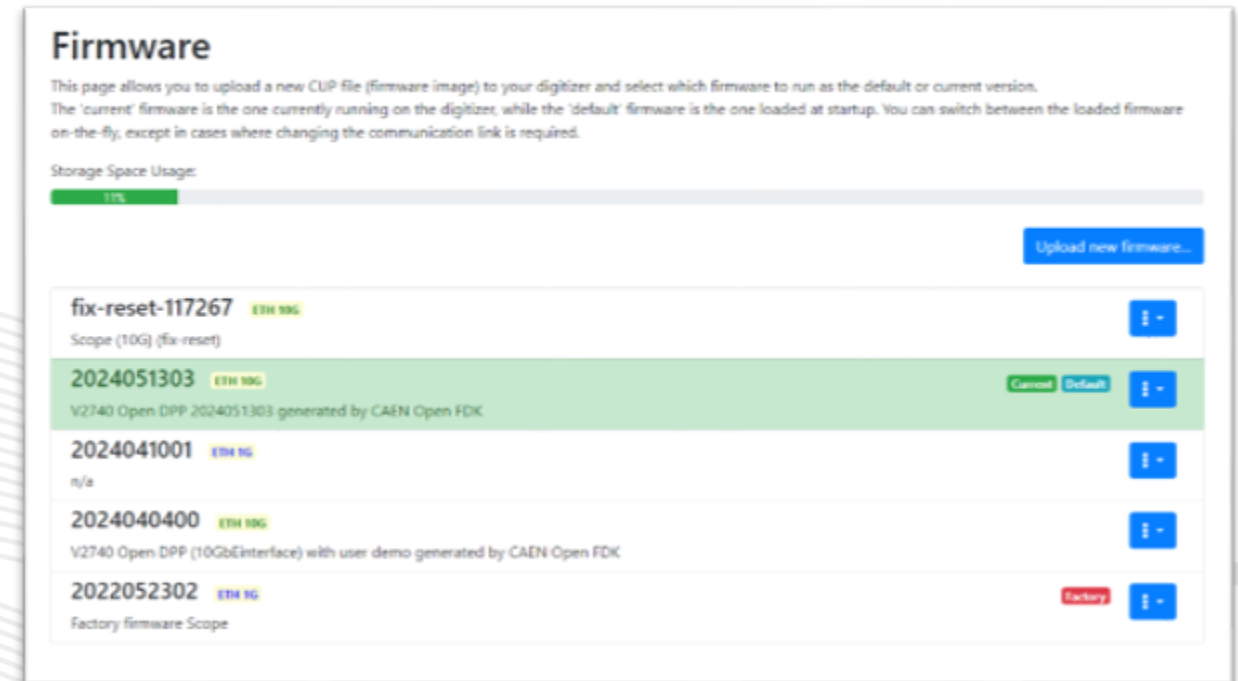
What's New

- Higher Channel Density
- Variable Gain Amplifier (VGA)
- Open-FPGA
- Fast Readout: up to 10 Gbps (~800 MB/s UDP)
- Up to 5 GB on-board memory
- Easier Scalability and Synchronization



Firmware Description

- Scope
- Digital Pulse Processing (DPP)
- Sci-Compiler
- Firmware Development Kit



Firmware

This page allows you to upload a new CUP file (firmware image) to your digitizer and select which firmware to run as the default or current version. The 'current' firmware is the one currently running on the digitizer, while the 'default' firmware is the one loaded at startup. You can switch between the loaded firmware on-the-fly, except in cases where changing the communication link is required.

Storage Space Usage:

10%

Upload new firmware...

fix-reset-117267	ETH 10G		
Scope (10G) (fix-reset)			
2024051303	ETH 10G	Current Default	
V2740 Open DPP 2024051303 generated by CAEN Open FDK			
2024041001	ETH 10G		
n/a			
2024040400	ETH 10G		
V2740 Open DPP (10GbEinterface) with user demo generated by CAEN Open FDK			
2022052302	ETH 10G	Factory	
Factory firmware Scope			

Firmware

- Scope
- Digital Pulse Processing (DPP)
- Sci-Compiler
- Firmware Development Kit



Firmware

- Scope
- Digital Pulse Processing (DPP)
- Sci-Compiler
- Firmware Development Kit



Firmware

- Scope
- Digital Pulse Processing (DPP)
- Sci-Compiler
- Firmware Development Kit

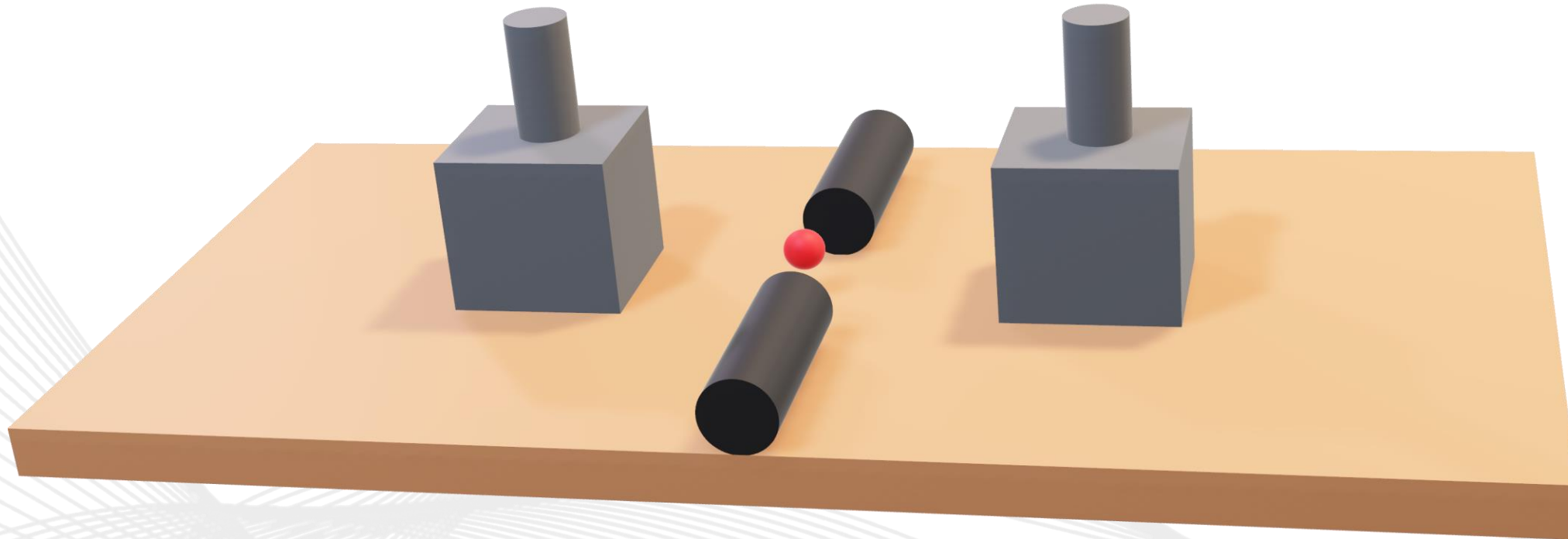


Firmware

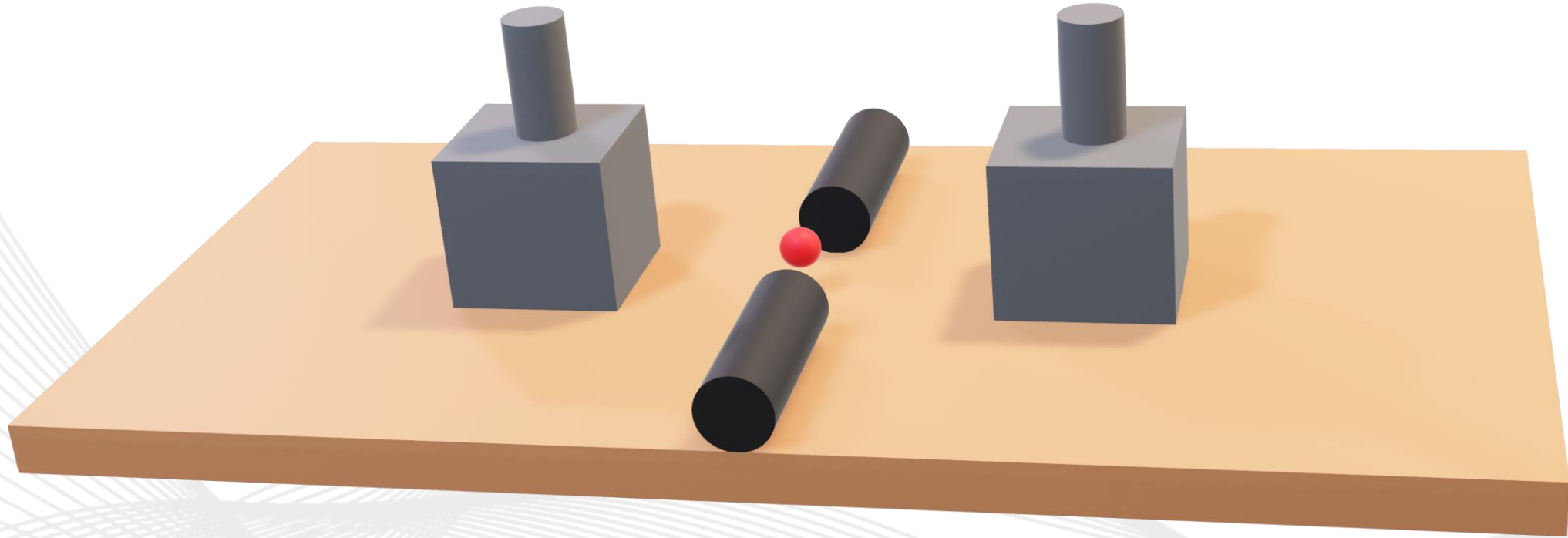
- Scope
- Digital Pulse Processing (DPP)
- Sci-Compiler
- Firmware Development Kit



Hands-On

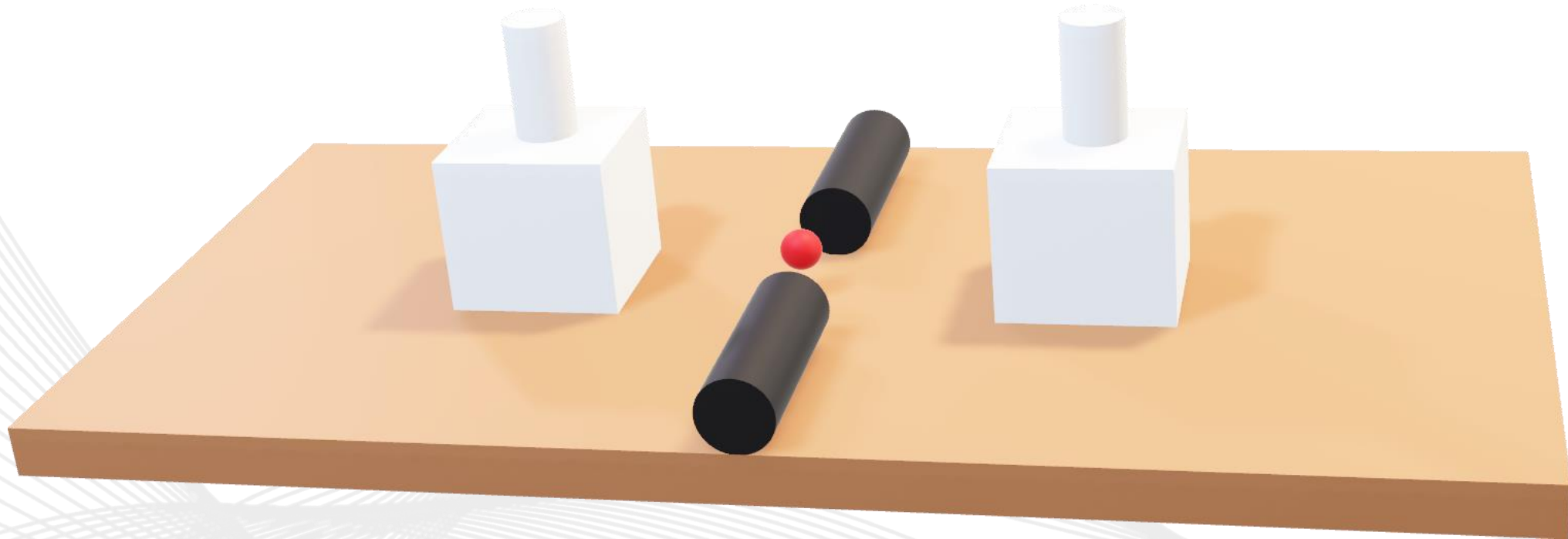


Hands-On



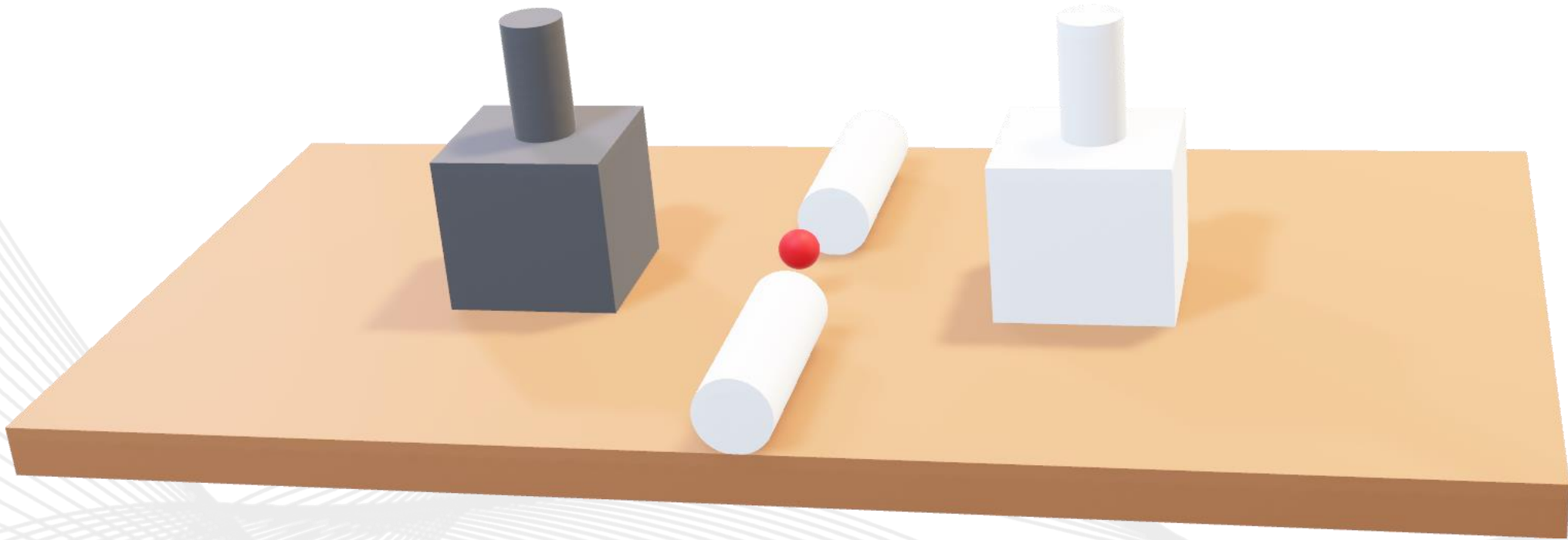
HV Bias : DT5790

Hands-On



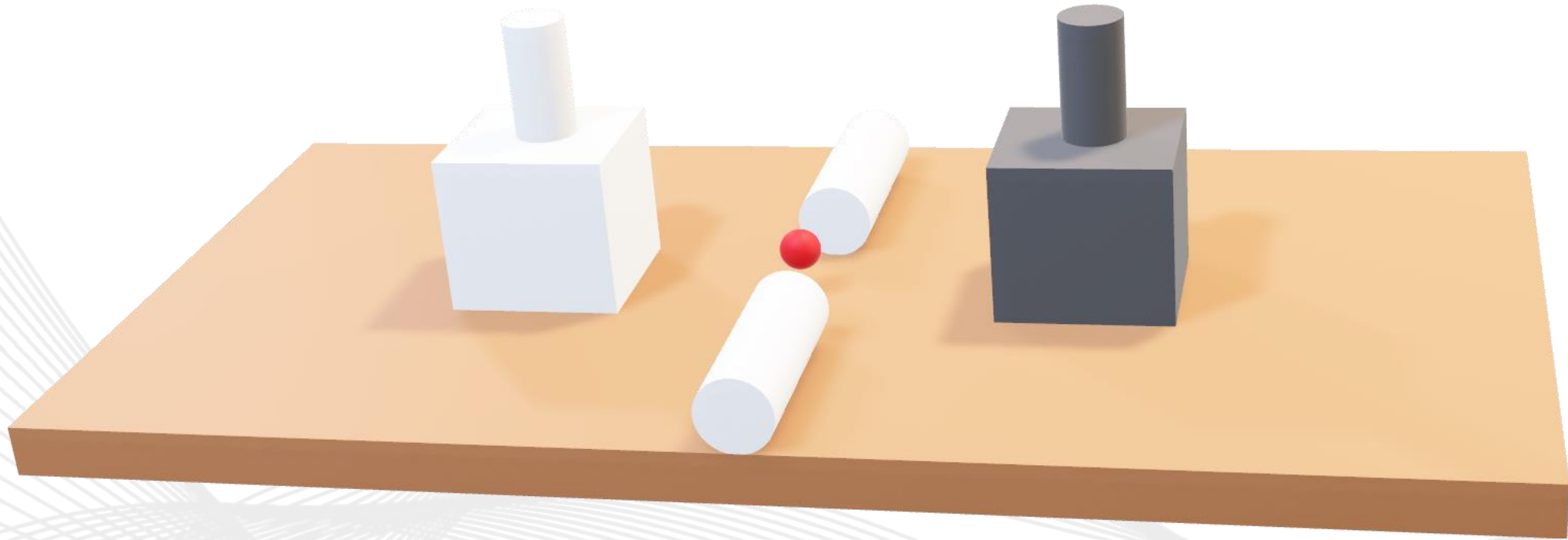
VX2730 DPP PSD

Hands-On



VX2740 DPP PHA + CSP (A1424)

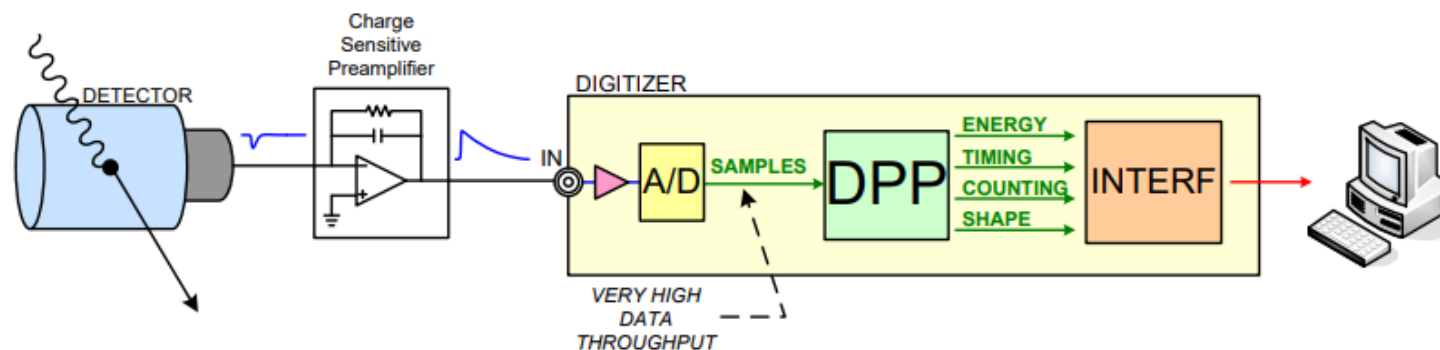
Hands-On



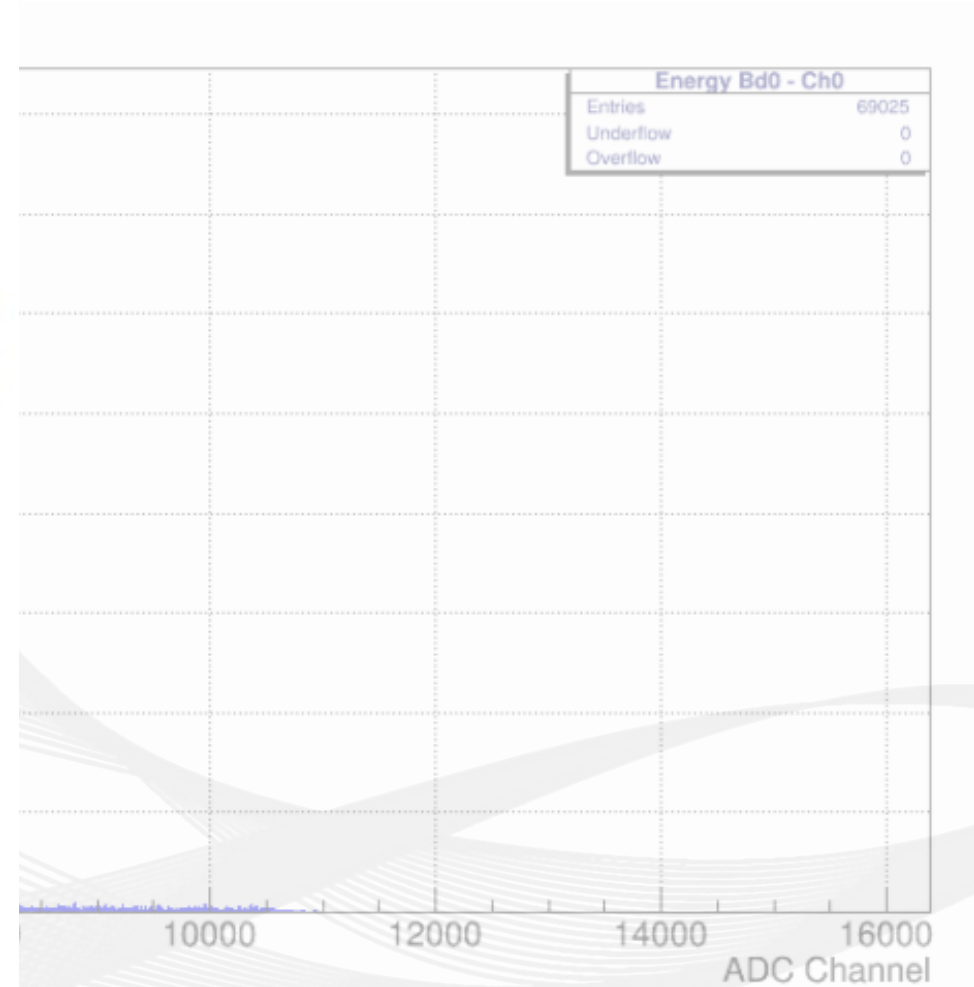
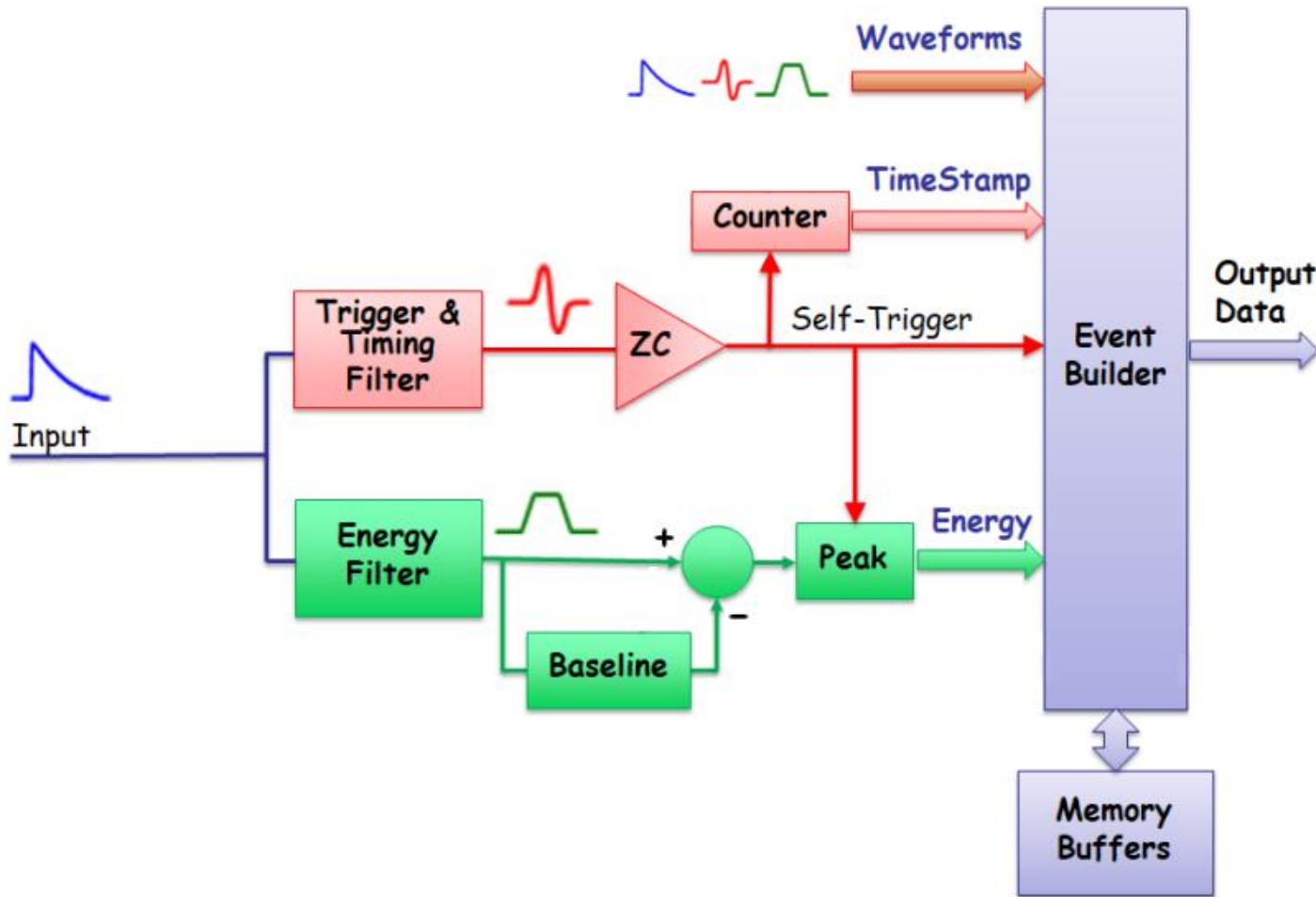
VX2740 DPP PHA

Pulse Height Analysis (PHA)

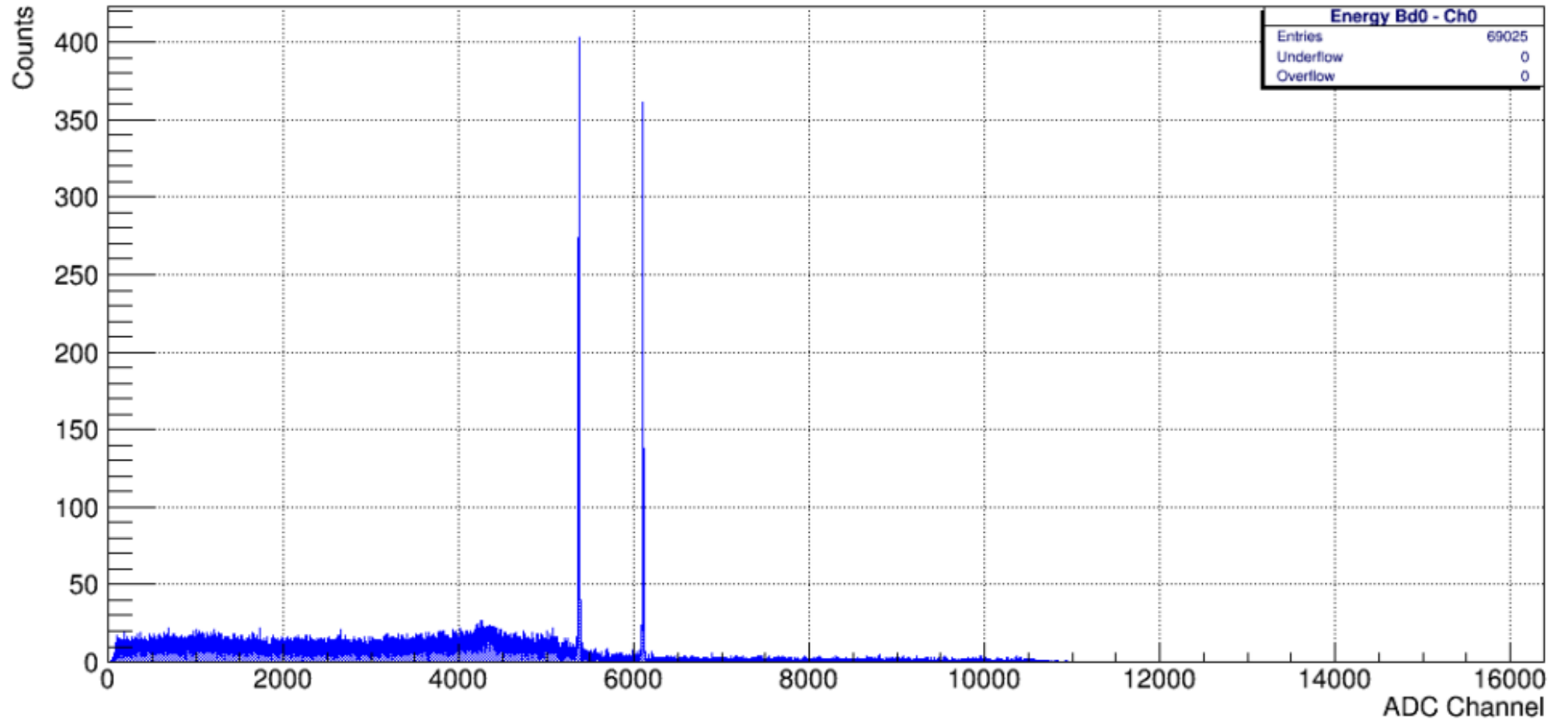
- Based on a Trapezoidal Filter
- Suited for CSP Signals
- Suited for direct Exponential Signals
- Allows to obtain High Resolution Energy Measurements



Pulse Height Analysis (PHA)



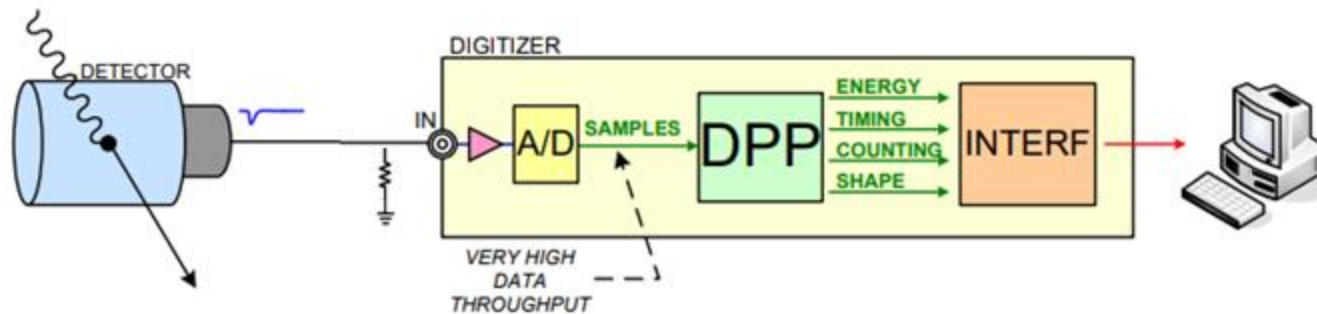
Pulse Height Analysis (PHA)



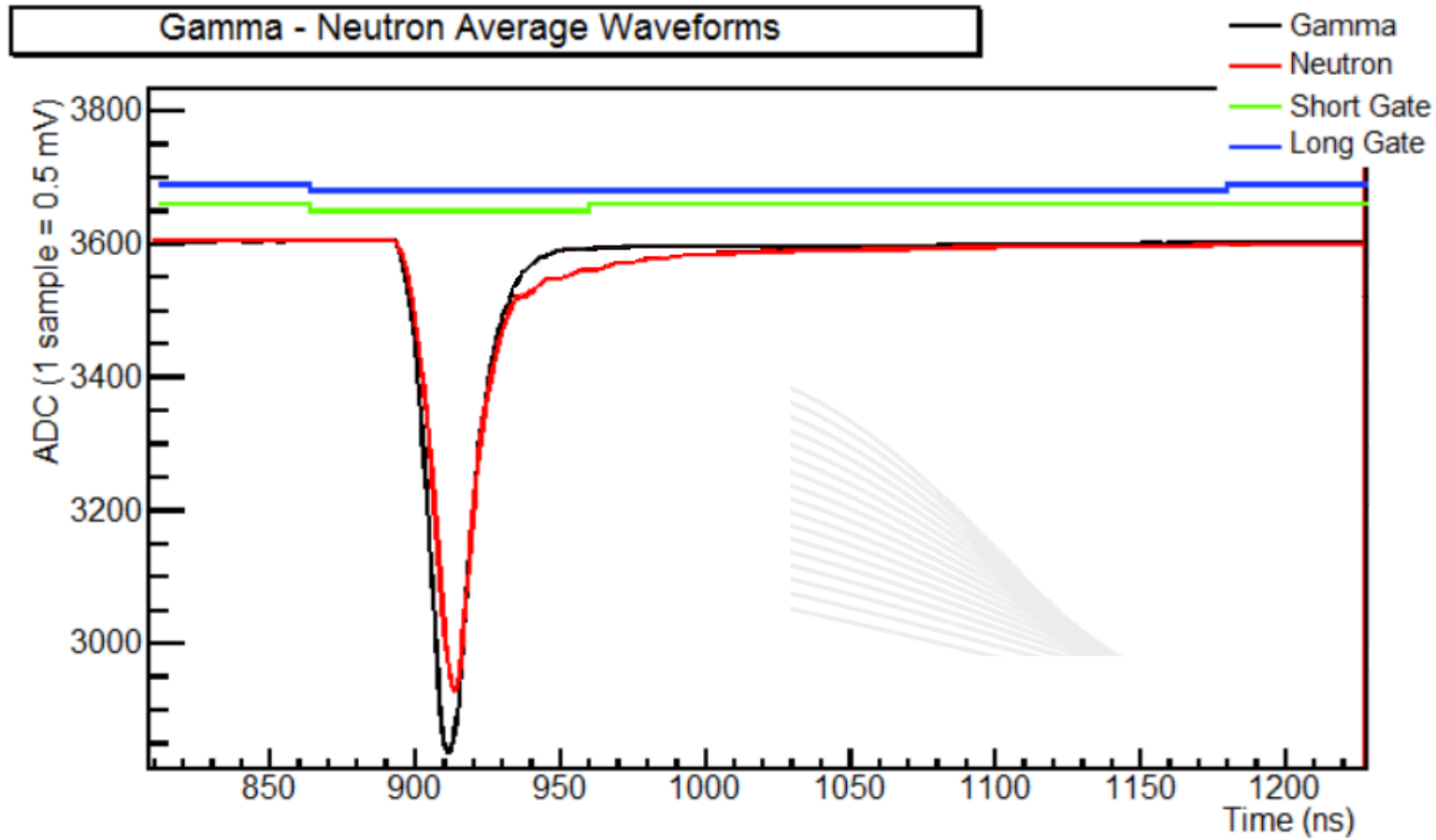
Input

Pulse Shape Discrimination (PSD)

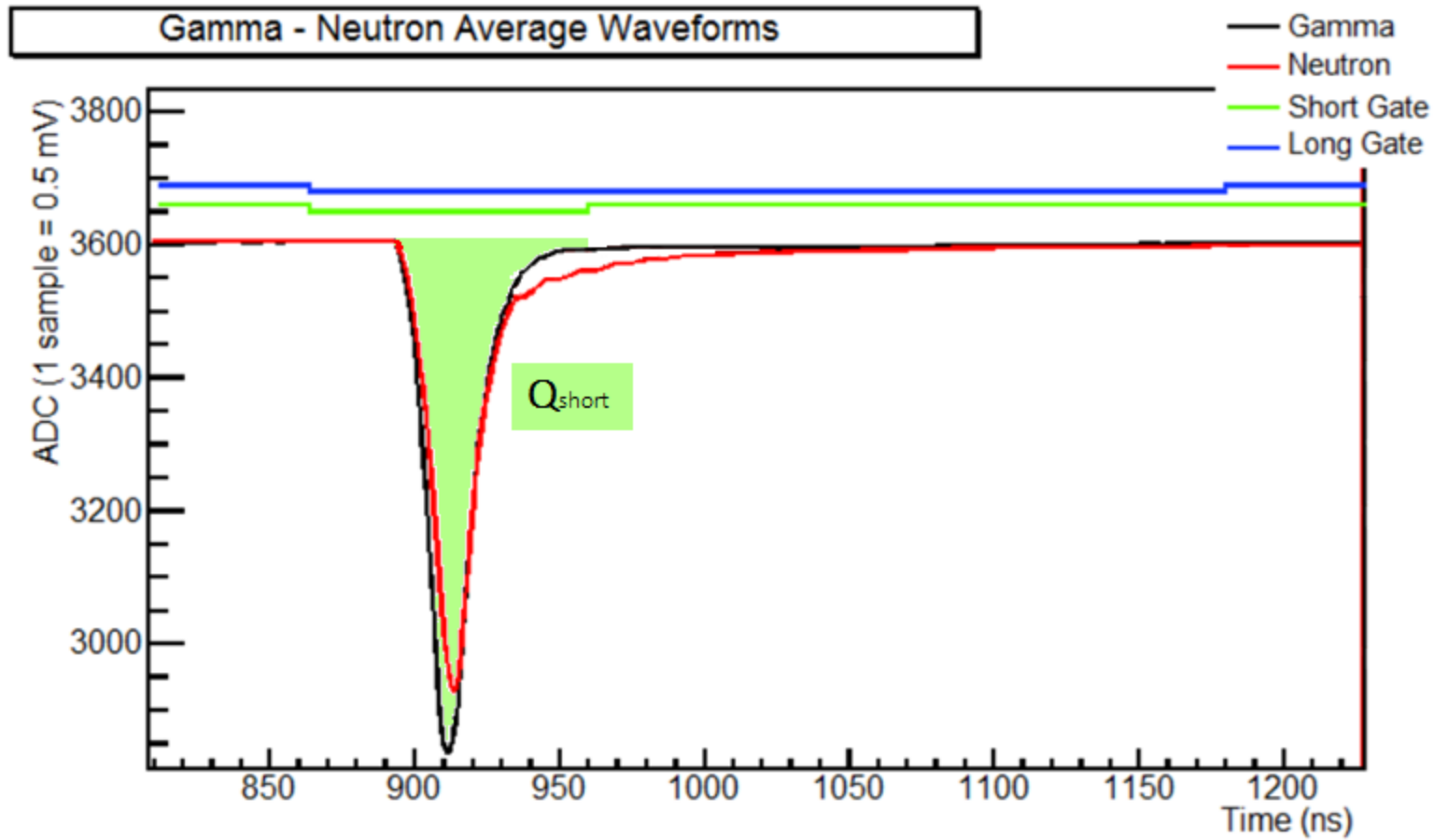
- Based on Signals from Particles with Different Specific Ionization
- Allows Charge Integration
- Allows Multiparametric Acquisition (Time + Energy + PSD)
- Suited for Direct Signals (no CSP)



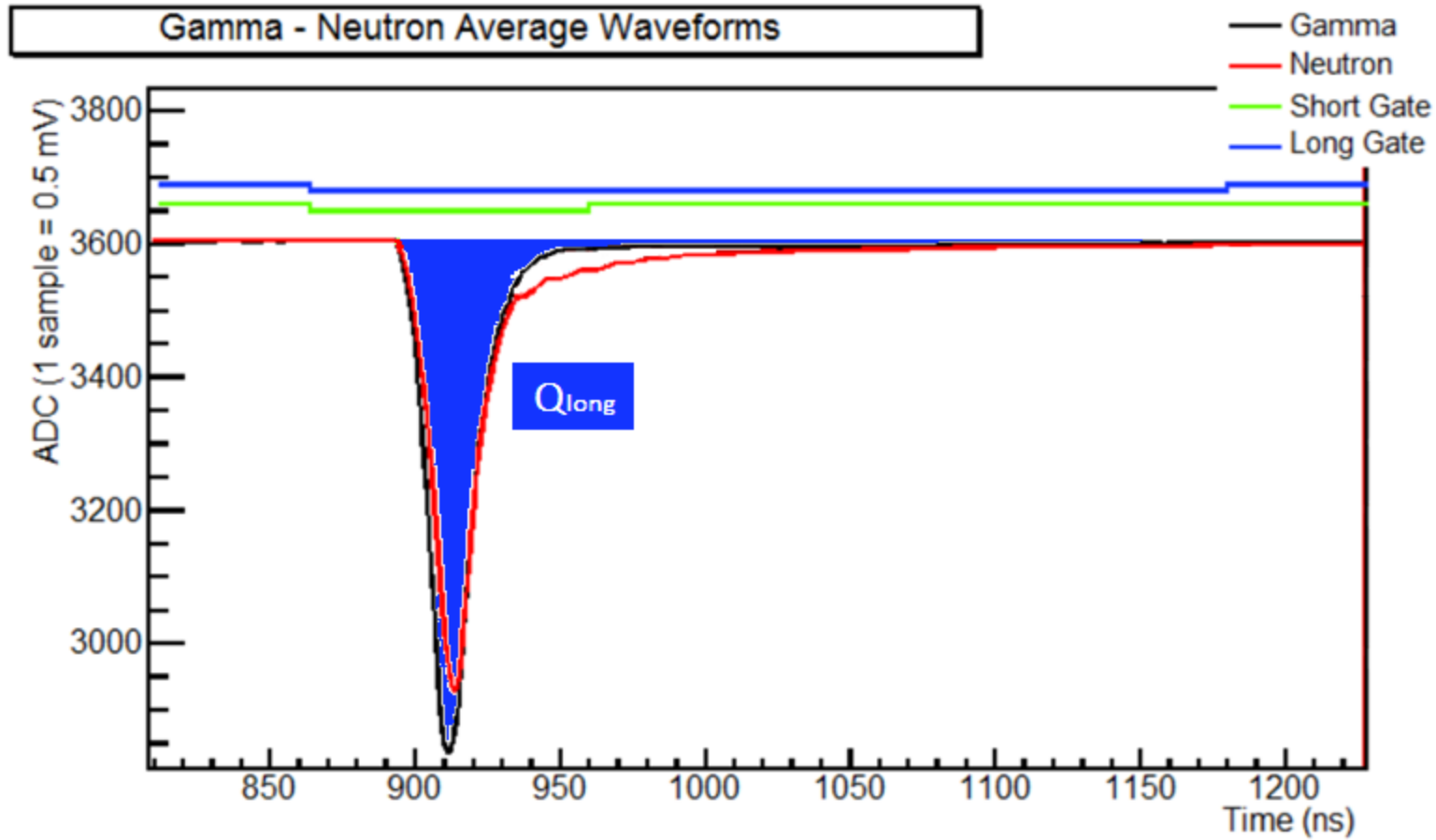
Pulse Shape Discrimination (PSD)



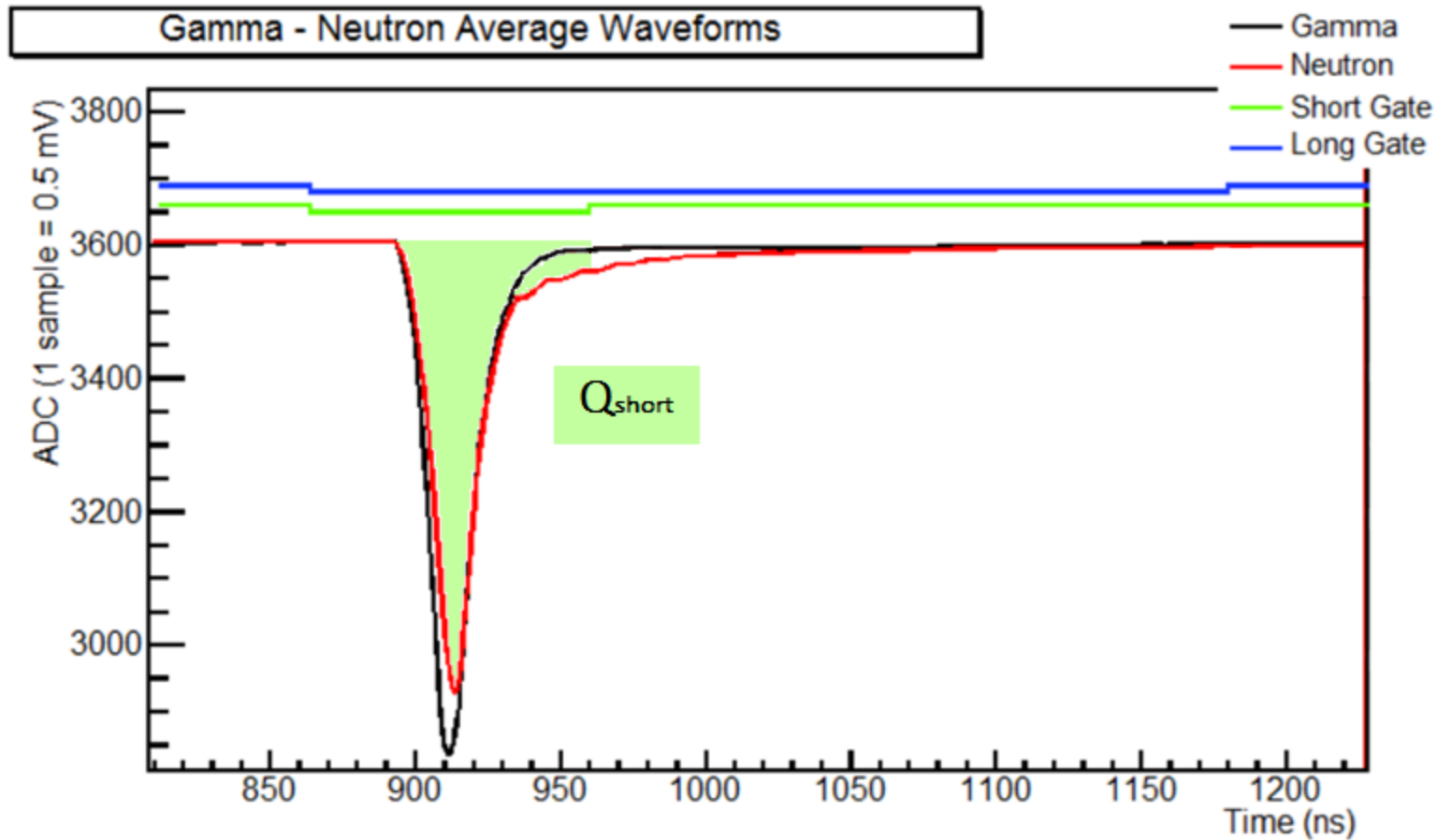
Pulse Shape Discrimination (PSD)



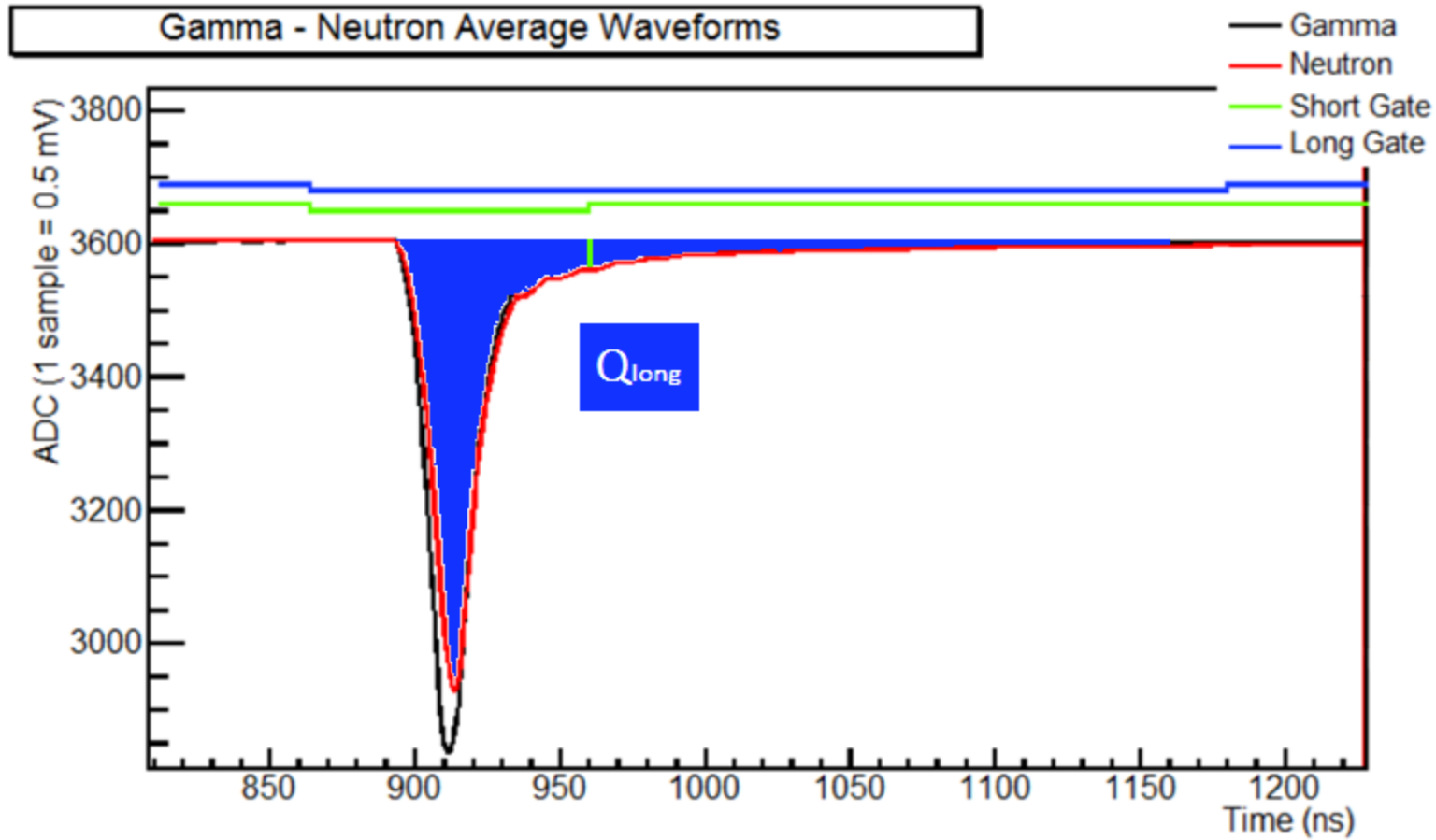
Pulse Shape Discrimination (PSD)



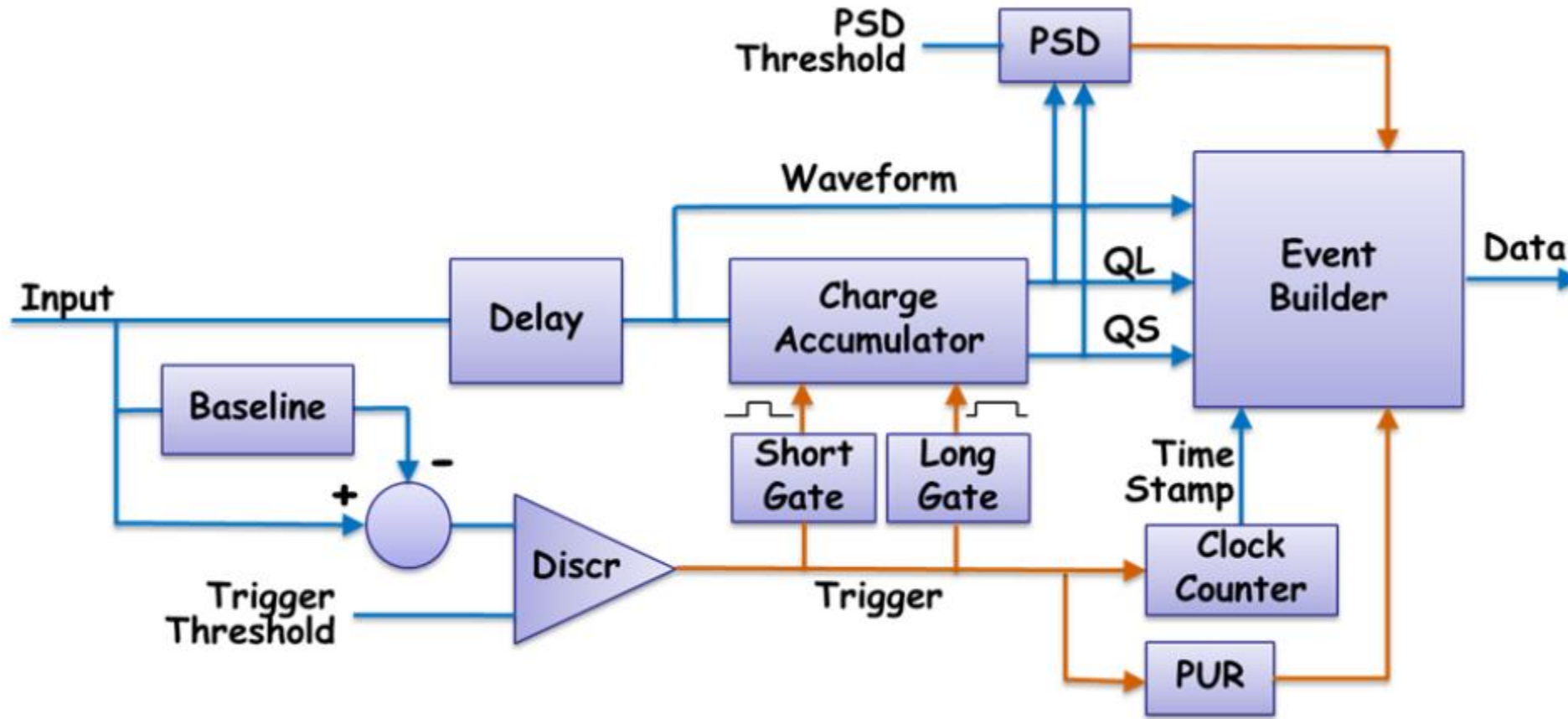
Pulse Shape Discrimination (PSD)



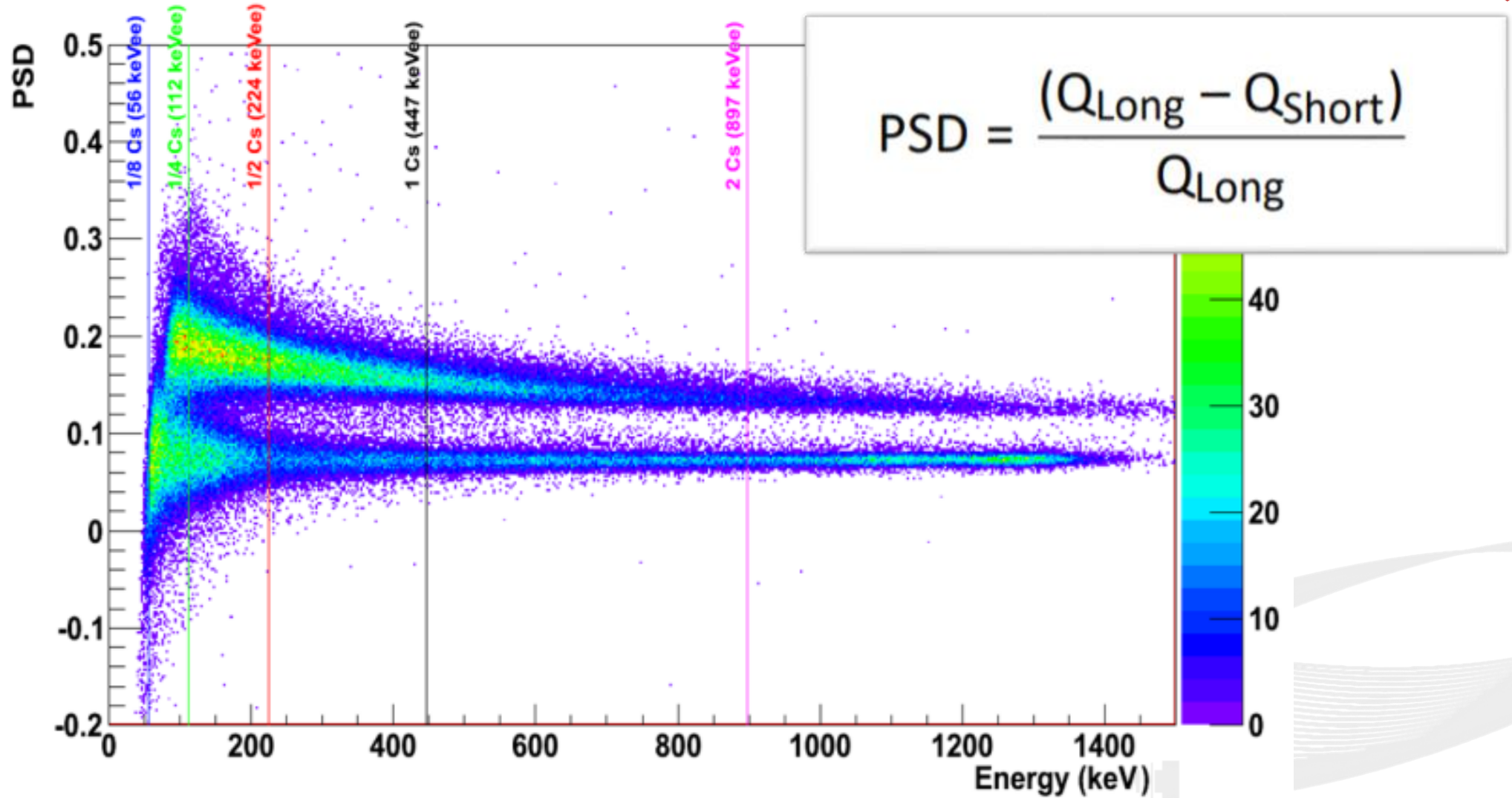
Pulse Shape Discrimination (PSD)



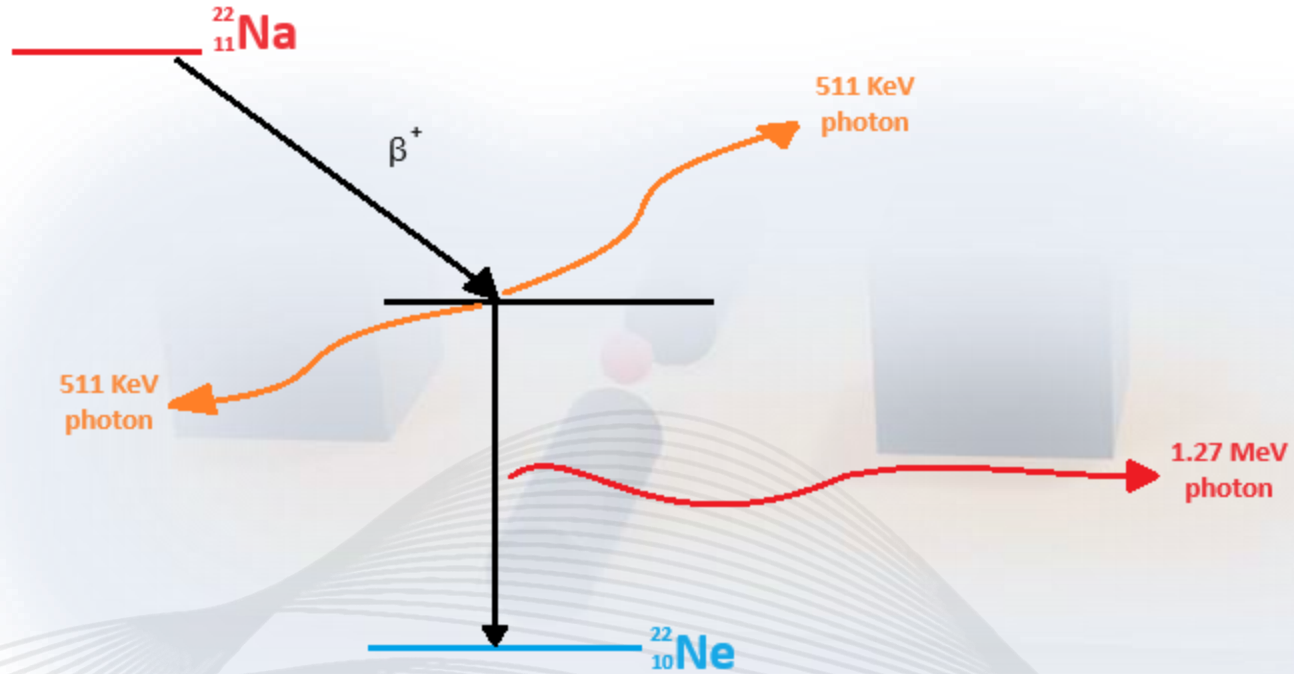
Pulse Shape Discrimination (PSD)



Pulse Shape Discrimination (PSD)



Na22 Decay Scheme

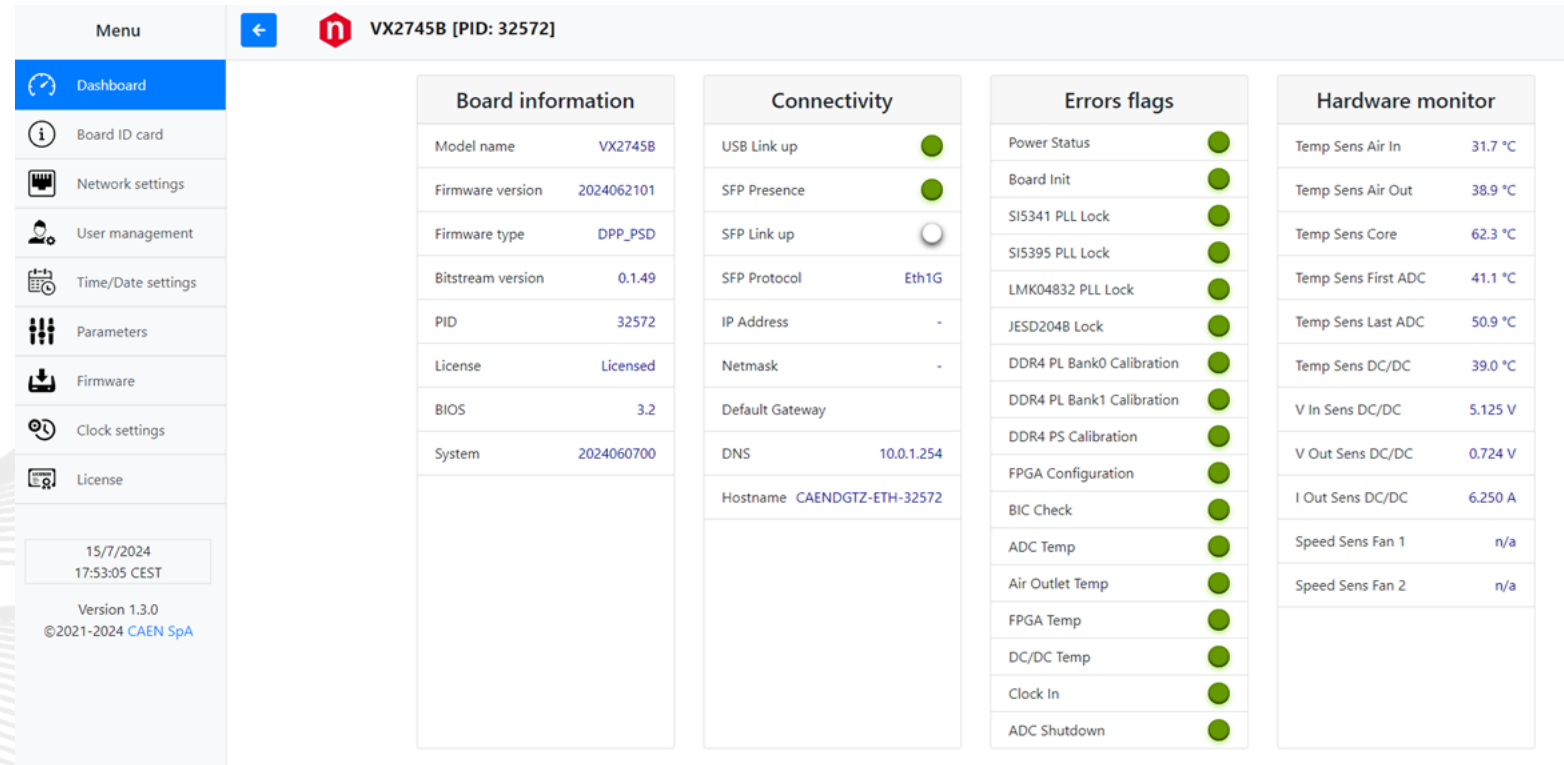



$\text{NaI} + \text{BaF}_2$

Thank you!

Digitizer's Web Interface

- Board information and status
- Network configuration
- Firmware upgrade
- License manager
- Clock settings
- Parameters page



Menu ←  VX2745B [PID: 32572]

Board information	Connectivity	Errors flags	Hardware monitor
Model name: VX2745B	USB Link up: ●	Power Status: ●	Temp Sens Air In: 31.7 °C
Firmware version: 2024062101	SFP Presence: ●	Board Init: ●	Temp Sens Air Out: 38.9 °C
Firmware type: DPP_PSD	SFP Link up: <input type="checkbox"/>	SI5341 PLL Lock: ●	Temp Sens Core: 62.3 °C
Bitstream version: 0.1.49	SFP Protocol: Eth1G	SI5395 PLL Lock: ●	Temp Sens First ADC: 41.1 °C
PID: 32572	IP Address: -	LMK04832 PLL Lock: ●	Temp Sens Last ADC: 50.9 °C
License: Licensed	Netmask: -	JESD204B Lock: ●	Temp Sens DC/DC: 39.0 °C
BIOS: 3.2	Default Gateway: -	DDR4 PL Bank0 Calibration: ●	V In Sens DC/DC: 5.125 V
System: 2024060700	DNS: 10.0.1.254	DDR4 PL Bank1 Calibration: ●	V Out Sens DC/DC: 0.724 V
	Hostname: CAENDGTZ-ETH-32572	DDR4 PS Calibration: ●	I Out Sens DC/DC: 6.250 A
		FPGA Configuration: ●	Speed Sens Fan 1: n/a
		BIC Check: ●	Speed Sens Fan 2: n/a
		ADC Temp: ●	
		Air Outlet Temp: ●	
		FPGA Temp: ●	
		DC/DC Temp: ●	
		Clock In: ●	
		ADC Shutdown: ●	

15/7/2024
17:53:05 CEST

Version 1.3.0
©2021-2024 CAEN SpA

WaveDump 2

- C++ software for CAEN Digitizer 2.0 running FW Scope
- User-friendly GUI
- Multi-board management
- Simultaneous plot of waveforms
- FFT and Samples Histogram provided runtime
- Data saving (ASCII or binary format)
- Import/Export of configuration presets

